What is Claimed:

1. A process for fabricating an electronic device, the process comprising:

(a.) forming a first dopant blocking layer at a first temperature; and

(b.) forming a second dopant blocking layer at a second temperature over said first dopant blocking layer.

2. A process as recited in claim 1, wherein said first temperature is lower than said second temperature.

3. A process as recited in claim 1, wherein the process further comprises:

forming a third dopant blocking layer between said first and said second dopant blocking layers.

4. A process as recited in claim 1, wherein said first dopant blocking layer is formed over a vertical sidewall of a mesa and over a horizontal surface of a substrate; and

said first dopant blocking layer has a substantially uniform thickness.

5. A process as recited in claim 1, wherein said first and said second blocking layers are InAlAs.

6. A process as recited in claim 3, wherein said third dopant blocking layer is chosen from the group consisting essentially of InP, InGaP, InGaAs, or InGaAsP.

7. A process as recited in claim 1, wherein said first temperature lies in the range of approximately 500°C to approximately 570°C.

8. A process as recited in claim 4, wherein said thickness is in the range of approximately 50 nm to approximately 100 nm.

9. A process as recited in claim 1, wherein said second dopant blocking layer has a vertical portion and said vertical portion has a thickness in the range of approximately 30 nm to approximately 100 nm.

10. A process as recited in claim 1, wherein said first and second dopant blocking layers are InGaAlAs.

11. A process as recited in claim 1, wherein said first dopant blocking layer is disposed above a p-type layer and said second dopant blocking layer is disposed below a semi-insulating layer.

12. A process a recited in claim 1, wherein said first dopant blocking layer is disposed below a p-type layer and said second dopant blocking layer is disposed above a semi-insulating layer.

13. A process for fabricating an optoelectronic device as recited in claim 1, wherein said second temperature lies in the range of approximately 600° C to approximately 650° C.

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14. A process as recited in claim 1, wherein said first and said second dopant barrier layers are formed by MOVPE.

15. A process as recited in claim 1, wherein said first and said second dopant barrier layers are formed by MBE.

16. A process as recited in claim 15, wherein said first temperature lies in the range of approximately 400° C to approximately 470° C.

17. A process as recited in claim 15, wherein said second temperature lies in the range of approximately 500° C to approximately 550° C.

18. A process as recited in claim 14, wherein said first temperature is in the range of approximately 500°C to approximately 570° C.

19. A process as recited in claim 14, wherein said second temperature lies in the range of approximately 600 °C to approximately 650 °C.

20. A process for fabricating an electronic device, the process comprising:

(a.) forming a first InAlAs layer at a first temperature; and

(b.) forming a second InAlAs layer at a second temperature over said first InAlAs layer.

21. A process as recited in claim 20, wherein said first temperature is lower than said second temperature.

22. A process as recited in claim 20, wherein the process further comprises:

forming a layer of undoped InP between said first and said second InAlAs layers.

23. A process as recited in claim 20, wherein said first InAlAs layer is formed over a vertical sidewall of a mesa and over a horizontal surface of a substrate; and

wherein said first InAlAs layer has a substantially uniform thickness.

24. A process as recited in claim 20, wherein said first InAlAs layer is disposed above a p-type layer and said second InAlAs layer is disposed below a semi-insulating layer.

25. A process a recited in claim 20, wherein said first InAlAs layer is disposed below a p-type layer and said second InAlAs layer is disposed above a semi-insulating layer.

26. A process for fabricating an electronic device as recited in claim 20, wherein said second temperature lies in the range of approximately 600 °C to approximately 650 °C.

27. A process as recited in claim 20, wherein said first temperature lies in the range of approximately 500 °C to approximately 570 °C.

28. A process as recited in claim 20, wherein said first and said second dopant blocking layers are formed by MOVPE.

29. A process as recited in claim 20, wherein said first temperature lies in the range of approximately 400 °C to approximately 470 °C.

30. A process as recited in claim 20, wherein said second temperature lies in the range of approximately 500° C to approximately 550° C.

31. A process as recited in claim 20 wherein said first and said second dopant blocking layers are formed by MBE.

32. An electronic device, comprising:

a multilayer dopant barrier disposed between a first doped layer and a second doped layer, said multilayer dopant barrier further comprising:

a first dopant blocking layer disposed adjacent said first doped layer; and

a second dopant blocking layer disposed adjacent said second doped layer.

33. An electronic device as recited in claim 32, wherein said first doped layer is in a mesa, and said second doped layer disposed on at least one side of said mesa.

34. An electronic device as recited in claim 33, wherein said first dopant blocking layer has a vertical portion adjacent a vertical sidewall of said mesa and a horizontal portion above a substrate.

35. An electronic device as recited in claim 32, wherein said first dopant blocking layer substantially prevents dopants from diffusing out of said first doped layer.

36. An electronic device as recited in claim 32, wherein said second dopant blocking layer substantially blocks dopants from diffusing out of said second doped layer.

37. An electronic device as recited in claim 32, wherein said first dopant blocking layer is InAlAs.

38. An electronic device as recited in claim 32, wherein said second dopant blocking layer is InAlAs.

39. An electronic device as recited in claim 34, wherein said vertical portion and said horizontal portion have a substantially identical thickness.

40. An electronic device as recited in claim 32, wherein said first dopant blocking layer has a resistivity in the range of approximately 10^6 Ω–cm to approximately 10^9 Ω–cm.

41. An electronic device as recited in claim 32, wherein said second dopant blocking layer has a resistivity in the range of approximately 10^4 Ω–cm to 10^5 Ω–cm.

42. An electronic device as recited in claim 32, wherein said first doped layer is p-doped InP and said second doped layer is InP(Fe).

43. An electronic device as recited in claim 32, wherein said first dopant blocking layer substantially blocks Zn dopants and said second dopant blocking layer substantially blocks iron dopants.

44. An electronic device as recited in claim 32, wherein the electronic device is chosen from the group consisting essentially of light emitting and light detecting optoelectronic devices.

45. An electronic device as recited in claim 32, wherein said first and said second dopant blocking layers are InAlGaAs.

46. An electronic device as recited in claim 32, wherein said multi-layer dopant barrier further comprises:

a third dopant blocking layer disposed between said first and said second dopant blocking layers.

47. An electronic device as recited in claim 46, wherein said third dopant blocking layer is chosen from the group consisting essentially of InP, InGaP, InGaAs and InGaAsP.

48. An electronic device, comprising:

a multilayer dopant barrier disposed between a first doped layer and a second doped layer, said multilayer dopant barrier further comprising:

a first dopant blocking layer contiguous with said first doped layer; and

a second dopant blocking layer contiguous with said second doped layer.

49. An electronic device as recited in claim 48, wherein said first doped layer is in a mesa, and said second doped layer is disposed on at least one side of said mesa.

50. An electronic device as recited in claim 49, wherein said first dopant blocking layer has a vertical portion adjacent a vertical sidewall of said mesa and a horizontal portion above a substrate.

51. An electronic device as recited in claim 48, wherein said first dopant blocking layer substantially prevents dopants from diffusing out of said first doped layer.

52. An electronic device as recited in claim 48, wherein said second dopant blocking layer substantially blocks dopants from diffusing out of said second doped layer.

53. An electronic device as recited in claim 48, wherein said first and said second dopant blocking layers are InAlAs.

54. An electronic device as recited in claim 48, wherein said multi-layer dopant barrier further comprises:

a third dopant blocking layer disposed between said first and said second dopant blocking layers.

55. An electronic device as recited in claim 54, wherein said third dopant blocking layer is chosen from the group consisting essentially of InP, InGaP, InGaAs and InGaAsP.

56. An electronic device as recited in claim 48, wherein said first doped layer is p-type and said second doped layer is semi-insulating.

57. An electronic device as recited in claim 48, wherein said first and said second dopant blocking layers are InAlGaAs.

58. An electronic device as recited in claim 48, the electronic device is chosen from the group consisting essentially of light emitting and light detecting optoelectronic devices.

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